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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,255	07/15/2003	Tan Ping Chet	A943	9734

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EXAMINER	
MAGEE, THOMAS J	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 09/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/621,255	CHET ET AL.	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-25 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-8 and 10-25 is/are rejected.

7)☒ Claim(s) 9 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 07152003.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections – 35 U.S.C. 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 – 3, 10 – 13, 15, 18 - 20 and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Hamzehdoost et al. (US 5,491,362).

3. Regarding Claims 1 and 25, Hamzehdoost al. disclose an integrated circuit package comprising:

a die attach pad (208) (Figure 5)] having a first and second surface, the first and second surface being on opposite sides of the die attach pad,

an integrated circuit die (202) mounted on the first surface of the die attach pad, the integrated circuit die having a plurality of terminal pads (500) and

a substrate (See Appended Marked-up Figure 5)) mounted on the first surface, the substrate having an aperture, where the aperture encompasses the integrated circuit die, the substrate having a conductive band (226b) (layered conductor)

4. Regarding Claims 2 and 19, Hamzehdoost et al. disclose the presence of an opening (216) extending to the backside of the die (202) (Col. 5, lines 1 – 7) for a heat sink. Hamzehdoost et

al. disclose in Figure 8 that a heat sink plate (300) can be inserted at the back surface (Col. 6, lines 14 – 21) of a package, wherein, the second surface (204) of the die attach pad (208) is adjacent ("adjoining or in close proximity") to the heat sink formed in the cavity at 216.

5. Regarding Claim 3, Hamzehdoost et al. disclose, as discussed above, that the heat sink at 216 comprises a disk shape within the ring of 208.

6. Regarding Claim 10, Hamzehdoost et al. disclose that the integrated circuit die (202) is mounted on the die attach pad (208) using a thermally conductive electrically insulating adhesive (Col. 4, lines 63 – 65).

9. Regarding Claims 11 and 20, Hamzehdoost et al. disclose that a heat sink is attached to the die
attach pad with a heat-conductive adhesive material (Col. 6, lines 15 – 16). The plate at 216 is attached laterally to the die attach pad with the adhesive.

10. Regarding Claim 12, Hamzehdoost et al. disclose that the die is attached to the die attach pad with a thermally conductive (epoxy) adhesive. Although not explicitly disclosed, it would be apparent that the substrate would also be attached to the die attach pad with a thermally conductive adhesive and therefore, inherent.

11. Regarding Claims 13 and 15, Hamzehdoost et al. disclose (Col. 3, lines 31 – 35) that the conductive band (conductive layer) is connected to the internal lead fingers (PGA connector pins) (Col. 5, lines 20 – 24) using wire bonds (Col. 4, lines 14 – 20).

10. Regarding Claim 18, Hamzehdoost et al. disclose a method of packaging an integrated circuit comprising:

attaching an integrated circuit die (102) (Figure 5) on a die attach pad (208), the first and second surface being on opposite sides of the die attach pad, wherein the integrated circuit die (202) is mounted on the first surface of the die attach pad

mounting a substrate (See Appended marked-up Figure 5) on the first surface of the inserted die attach pad (208), the substrate having an aperture, where the aperture encompasses the integrated circuit die, the substrate having a conductive band (226b) between the outer edge of the substrate and the inner edge forming the aperture.

Claim Rejections – 35 U.S.C. 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art
are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hamzehdoost et al., as applied to Claims 1 – 3, 10 – 13, 15, 18 – 20, and 25, and further in view of Koike et al. (US 5,585,672).

13. Regarding Claim 4, Hamzehdoost et al. do not disclose the presence of a multi element heat sink structure having two disk shaped portions having a first disk shaped portion adjacent to the die attach pad and a second disk shaped portion adjacent the first disk, wherein the diameter of the first disk is greater than that of the second disk. Koike et al. disclose (Col. 2, lines 10 – 16) that the use of multiple heat sink plates increases heat transfer and reduces thermal damage. It would have then been obvious to one of ordinary skill in the art at the time of the invention to split the heat sink of Hamzehdoost et al. into a series of disks of varying material, whereby the second disk overlies the inserted die attach pad and the first disk (of greater diameter) overlies the first and is adjacent to the die attach pad to obtain better heat flow and less thermal damage, and thus to combine the multiple heat sink plate approach of Koike et al. with Hamzehdoost et al.

14. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hamzehdoost et al., as applied to Claims 1, 2, 6 – 8, 10 – 13, 15, 18 – 20, and 25, and further in view of Lawson et al. (US 5,912,804).

15. Regarding Claim 5, Hamzehdoost et al. do disclose that the heat sink comprises copper coated with nickel. Lawson et al. disclose as a part of prior art, nickel coated copper heat

sinks. It would have then been obvious to combine Lawson et al. with Hamzehdoost et al. to obtain efficient heat sinks of copper with a coating to prevent contamination of adjacent parts.

16. Claims 6 – 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamzehdoost et al., as applied to Claims 1 –3, 10 – 13, 15, 18 – 20, and 25, and further in view of Combs et al. (US 6,285,075 B1).

17. Regarding Claim 6, Hamzehdoost et al. do not disclose the presence of multiple bands on the substrate between the inner and outer edges. Combs et al. disclose (Col. 3, lines 24 – 29) the presence of a number of conductive bands (bonding planes) (113a – 113d) (Figure 1) along each of the edges of a rectangular substrate (112) between the inner edge forming the aperture and the outer edge. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Combs et al. with Hamzehdoost et al. to obtain a geometric arrangement of bonding planes (conductive bands) for ease of attachment of wires to bonding pads (See Figure 1, Combs et al.)

18. Regarding Claim 7, Hamzehdoost et al. do not disclose that the conduction band (226b) is a ground plane. Combs et al. disclose that the conductive planes (bonding planes) (113a – 113b) on a substrate form common ground planes. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Combs et al. and Hamzehdoost et al. to obtain a ground potential point for the integrated circuit.

19. Regarding Claim 8, Hamzehdoost et al. do not disclose a rectangular substrate with a substantially rectangular aperture having a plurality of conduction bands along each of the four edges of the substrate. Combs et al. disclose (Col. 3, lines 24 – 29) the presence of a number of conductive bands (bonding planes) (113a – 113d) (Figure 1) along each of the edges of a rectangular substrate (112) with a rectangular aperture. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Combs et al. with Hamzehdoost et al. to obtain a geometric arrangement of bonding planes (conductive bands) for ease of attachment of wires to bonding pads (See Figure 1, Combs et al.)

20. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hamzehdoost et al. as applied to Claims 1, 2, 6 – 8, 10 – 13, 15, 18 – 20, and 25, and further in view of Jacobi (US 4,842,662).

21. Regarding Claim 14, Hamzehdoost et al. do not disclose that the wire bonds are formed using copper wires coated with gold. Jacobi discloses the use of a thin copper conductor coated with gold for integrated circuit bonding connections (Col. 4, lines 17 – 18). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Jacobi and Hamzehdoost et al. to obtain efficient bonding of conductors to leads within the integrated circuit package.

22. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hamzehdoost et al., as applied to Claims 1, 2, 6 – 8, 10 – 13, 15, 18 – 20, and 25, and further in view of Newman et al. (US 6,225,685 B1).

23. Regarding Claim 16, Hamzehdoost et al. do not disclose a die attach pad that includes tie bar extensions. Newman et al. disclose (Col. 3, lines 4 – 7) a die attach pad (10) (Figure 1) with tie bar extensions (11). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Newman et al. with Hamzehdoost et al. to provide a die attach pad secured in the resin molding by tie bars (Newman, Col. 1, lines 13 – 17).

24. Claims 17, and 21 – 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamzehdoost et al., as applied to Claims 1, 2, 6 – 8, 10 – 13, 15, 18 – 20, and 25, and further in view of Baldwin (US 6,777,818 B2).

25. Regarding Claims 17 and 21, Hamzehdoost et al. do not disclose a data processing system containing processing circuitry with memory coupled to the processing circuitry and an integrated circuit die package. Baldwin discloses a data processing system (Figure 4) containing processing circuitry and an integrated circuit die package (46), wherein the integrated circuit die (of the type disclosed by Hamzehdoost et al.) is an ASIC (Col. 5, lines 4 – 10). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Baldwin with Hamzehdoost et al. to obtain a data processing system with an ASIC chip incorporated into the system.

26. Regarding Claim 22, Hamzehdoost et al. do not disclose that the integrated circuit package is mounted on a printed circuit board. Baldwin discloses (Col. 3, lines 16 – 31; Col. 4, lines 1 – 3) that the integrated circuit package (Figure 3) is mounted on a printed circuit board. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Baldwin with Hamzehdoost et al. to obtain a mounting base for the integrated circuit package.

27. Regarding Claims 23 and 24, Hamzehdoost et al. do not disclose a printed circuit board with processing circuitry and memory coupled to the integrated circuit package. Baldwin discloses, as discussed above, that the integrated circuit die is contained within a package (Figure 3) mounted on a printed circuit board (Col. 4, lines 1 – 3) that is contained within a data processing system (Figure 4) (Col. 4, lines 50 – 55), wherein processing circuitry (Figure 4) and memory (Figure 4) (Col. 5, lines 4 –10) and integrated circuit package are coupled. It would have then been obvious to one of ordinary skill in the art at the time of the invention to combine Baldwin and Hamzehdoost et al. to obtain an integrated circuit package that is incorporated into an electronic system for data processing.

Claim Objections

28. Claim 9 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and

any intervening claims. The prior art of record do not reasonably teach or suggest, either singularly or in combination, the limitation in Claim 9 of an integrated circuit package, wherein, "*the substrate comprises a dummy layer, a dielectric layer and a soldier mask structure encapsulating the dielectric layer and the soldier mask layer, a plurality of conductive bands in the soldier mask structure, the bands being separated by soldier mask material bands.*"

Conclusions

29. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(571) 272 1658.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Eddie Lee**, can be reached on **(571) 272-1732.** The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306.**

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Thomas Magee
August 24, 2004